

1 / 12

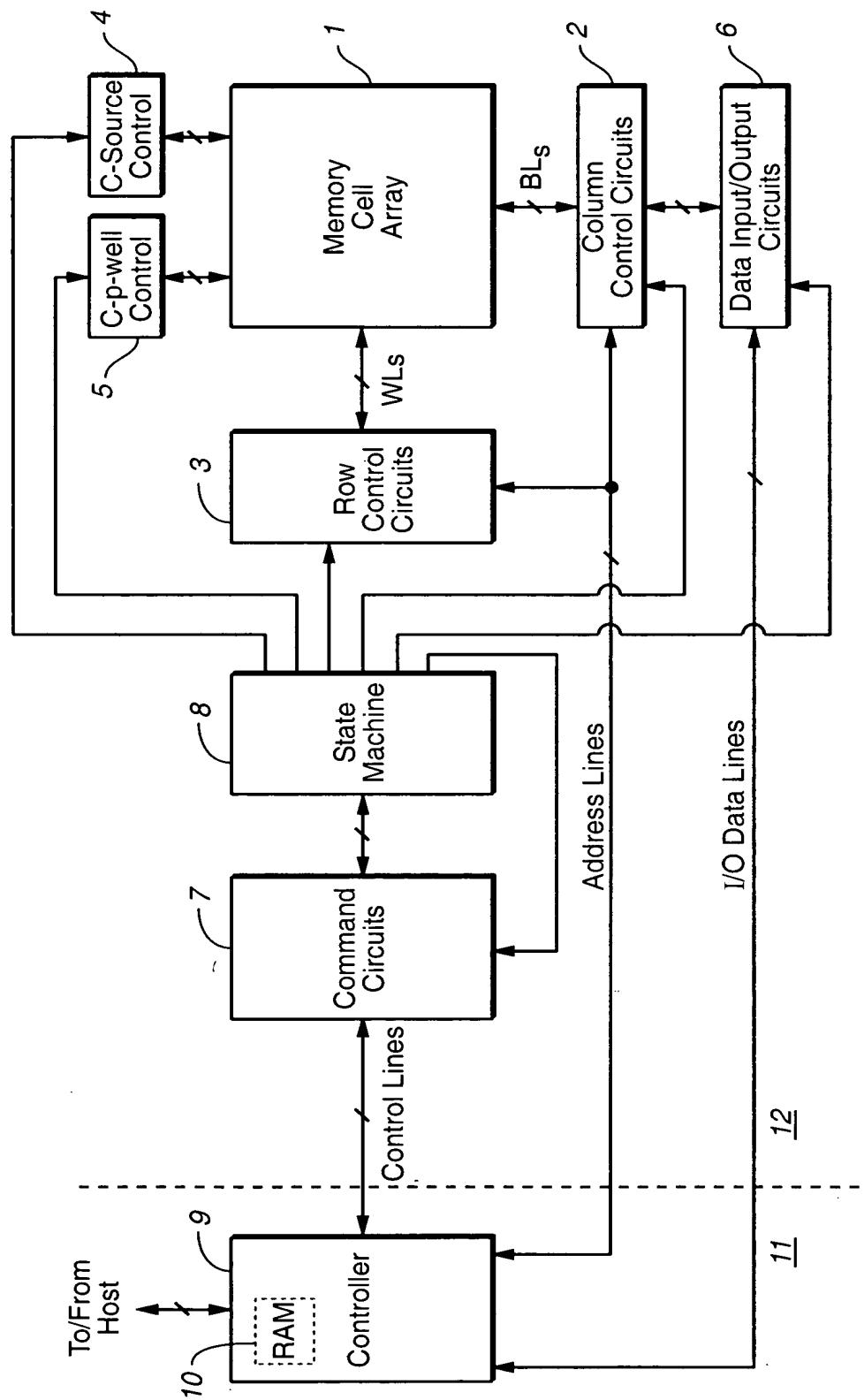


FIG. 1

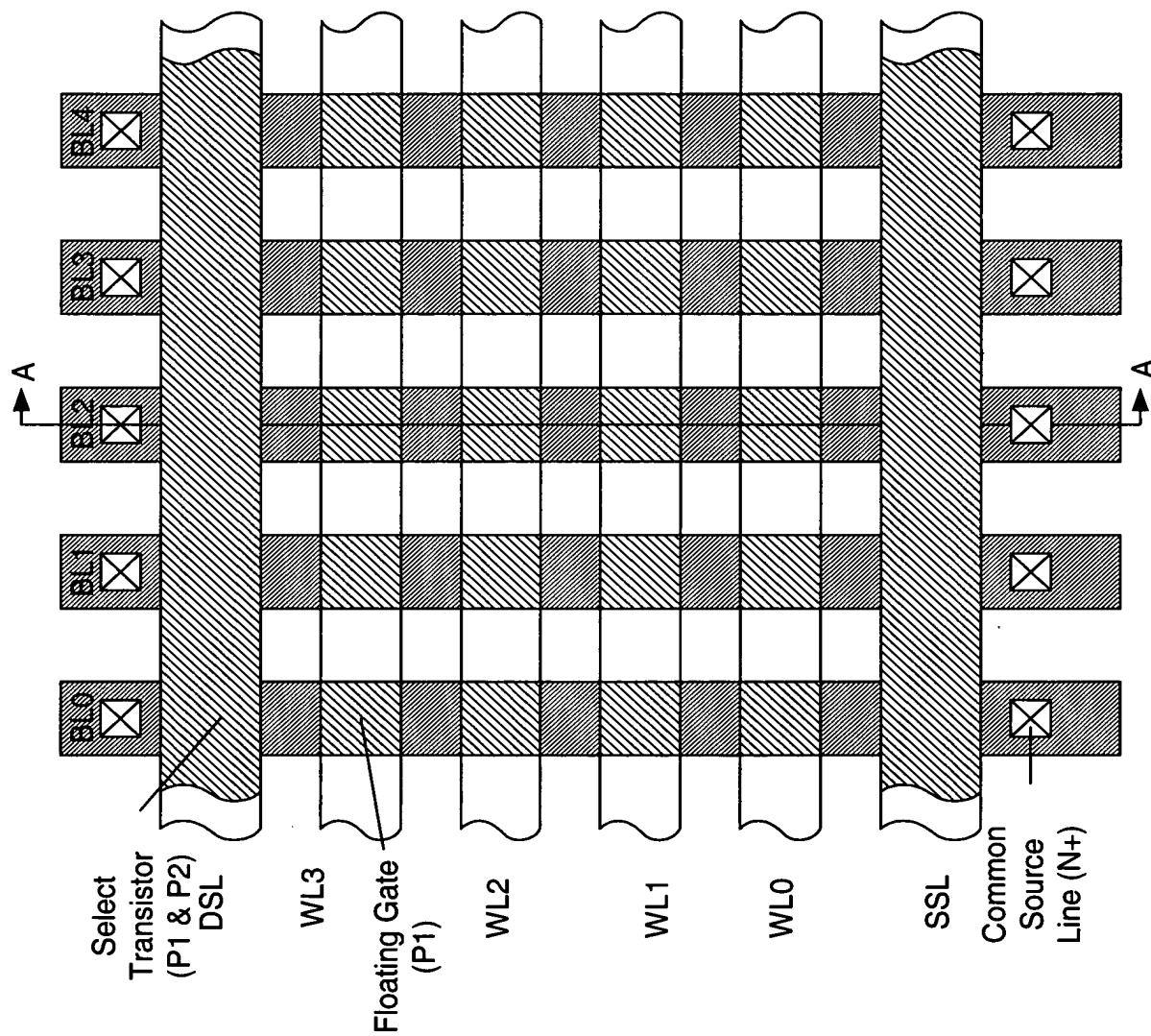


FIG.- 2A (PRIOR ART)

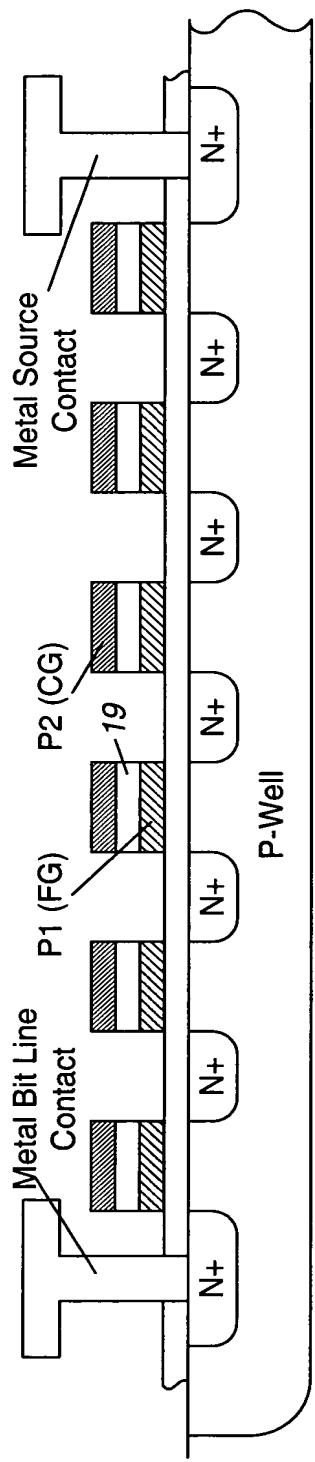


FIG. 2B (PRIOR ART)
(Section A-A)

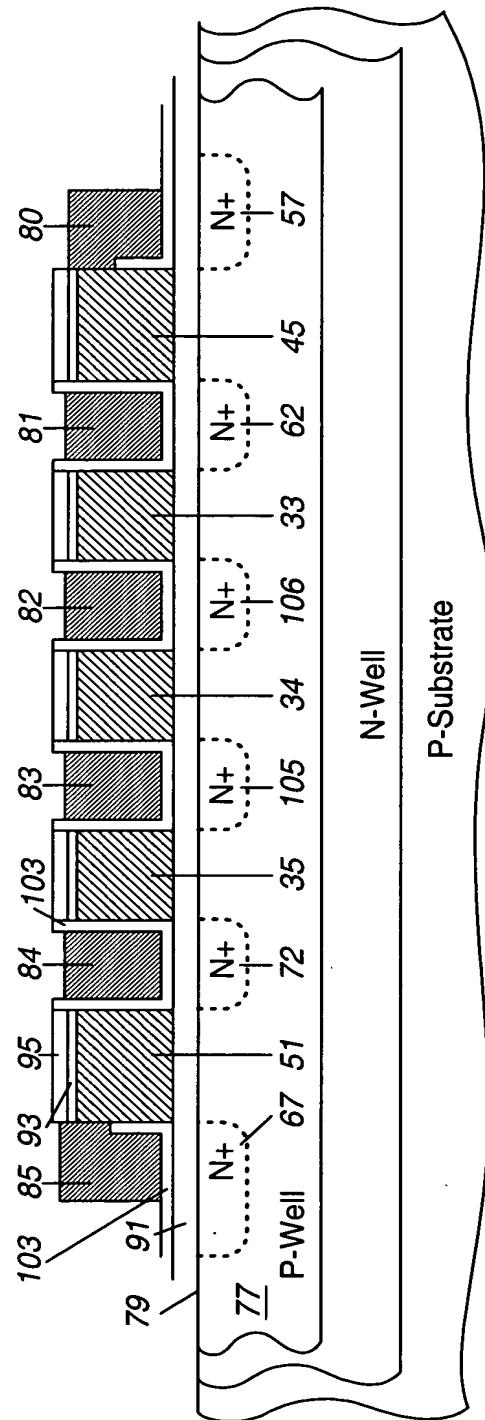


FIG. 4
(Section A-A)

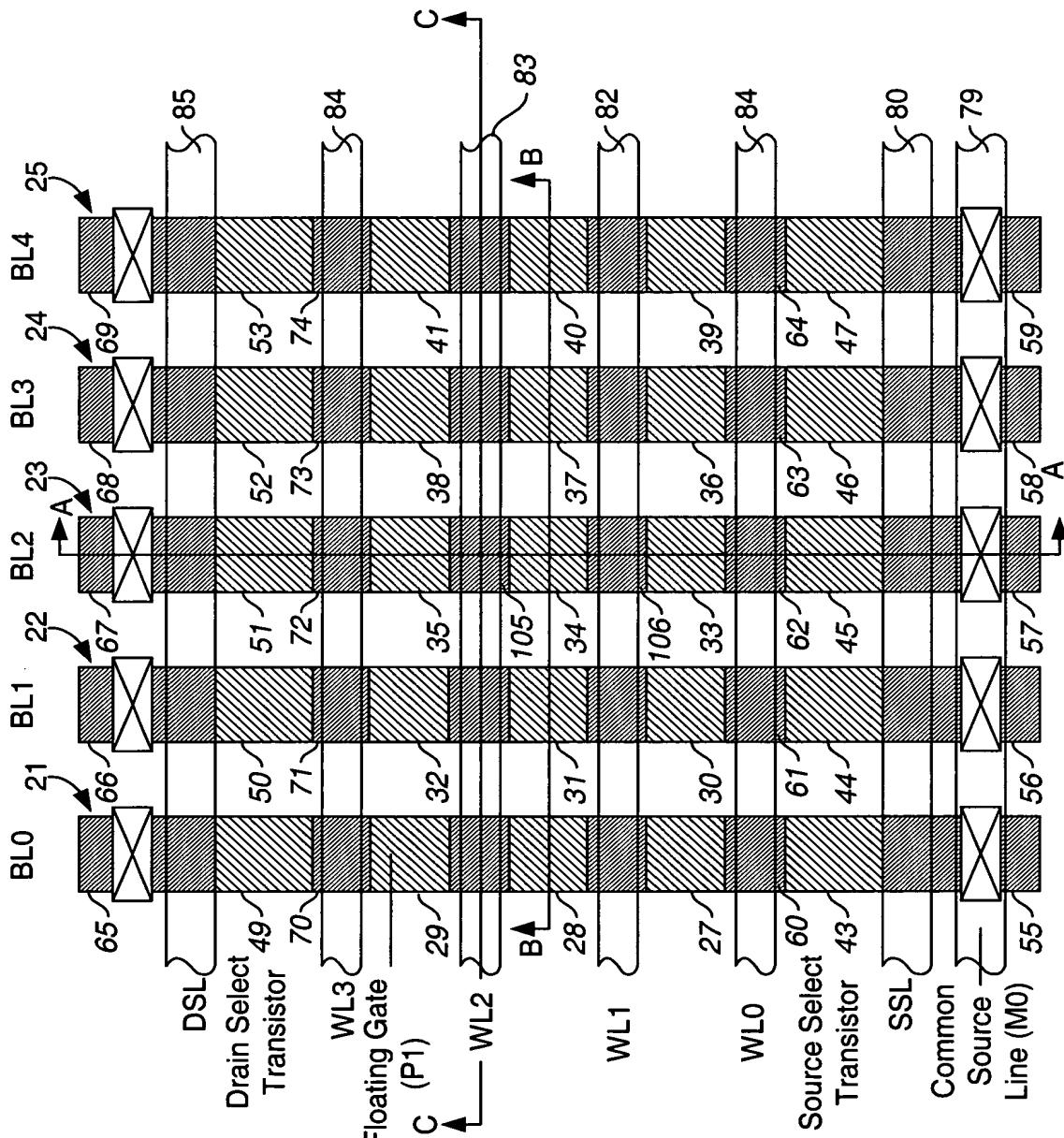


FIG. 3

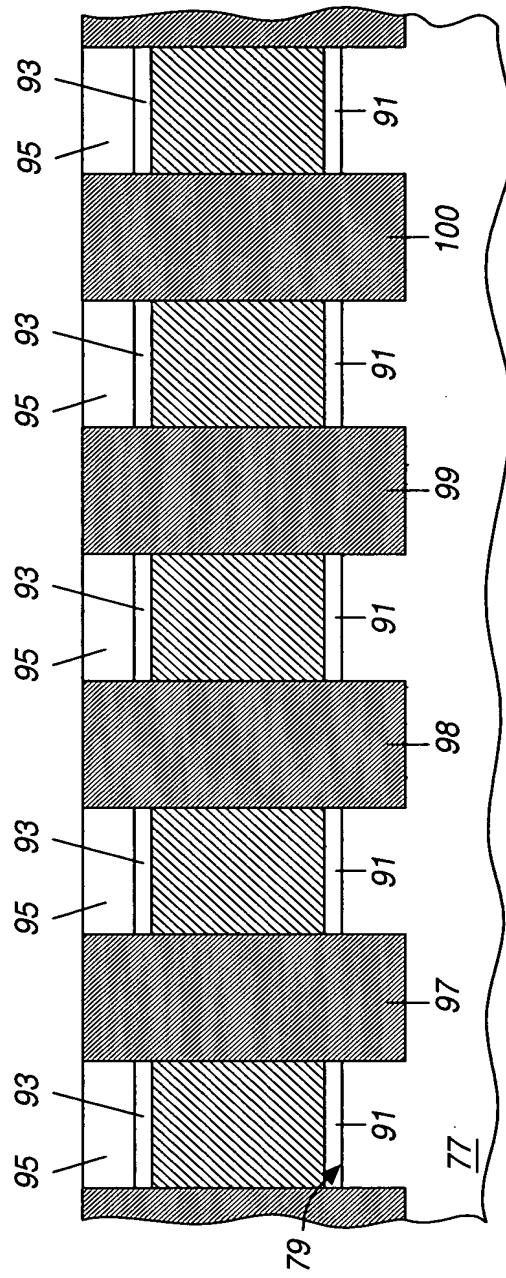


FIG. 5A
(Section B-B)

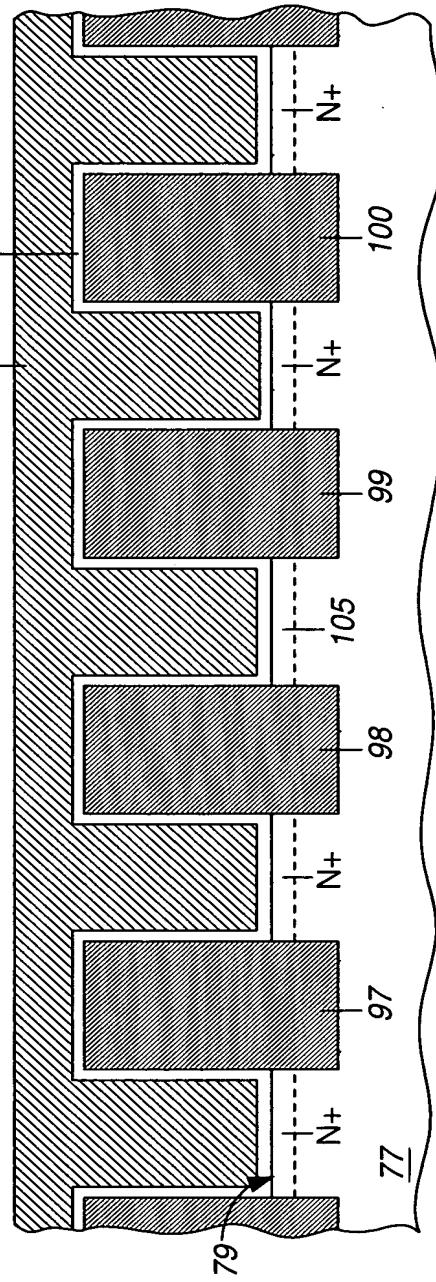


FIG. 5B
(Section C-C)

6 / 12

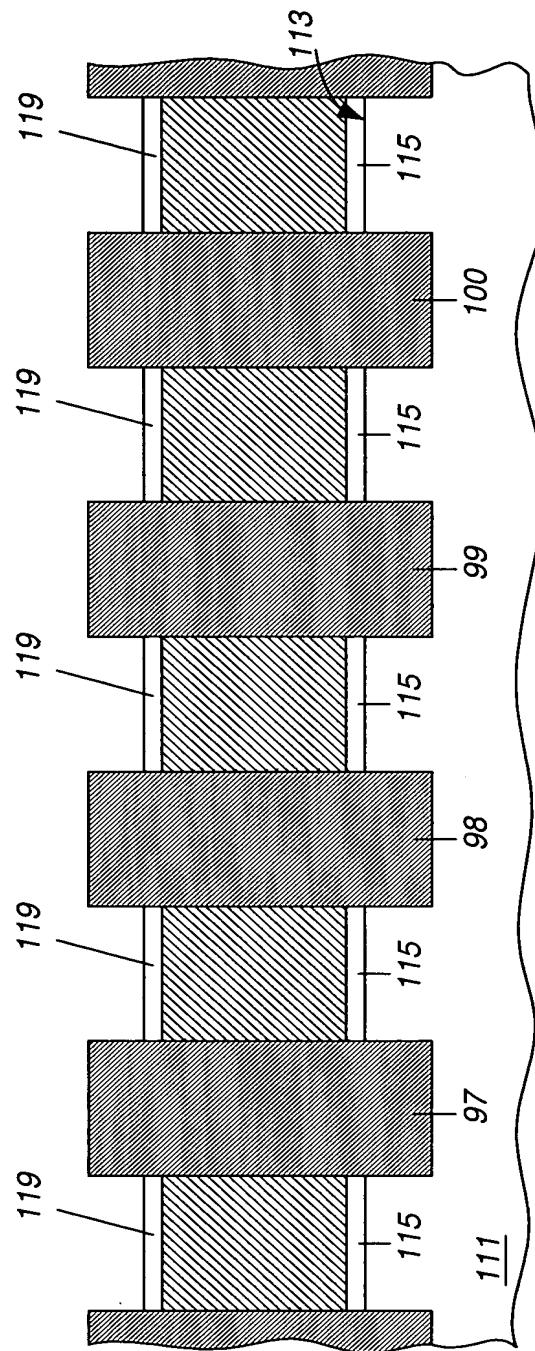
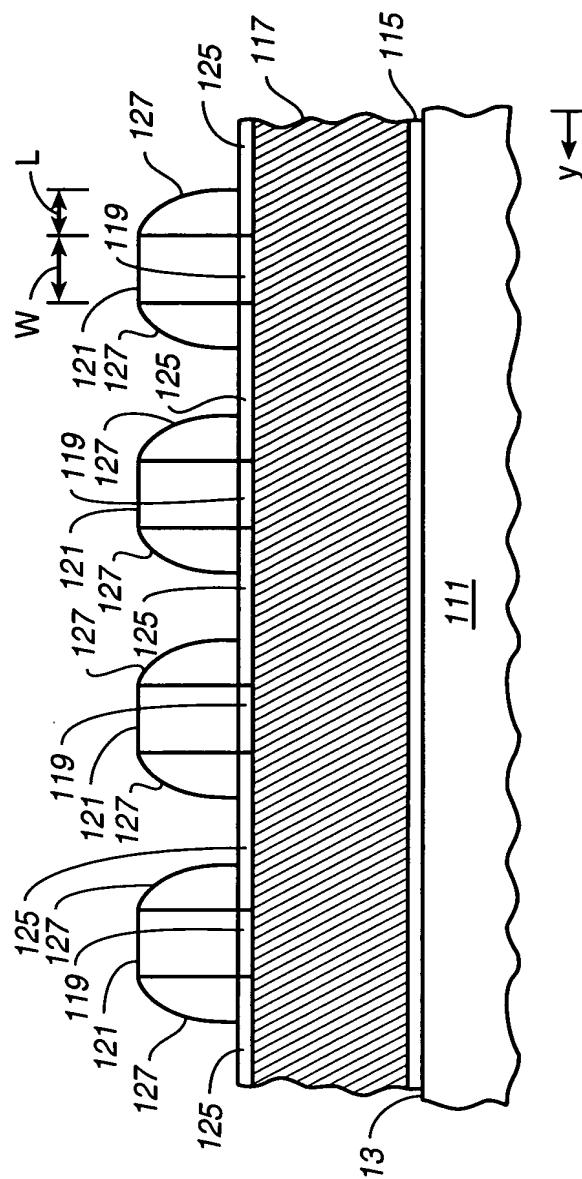
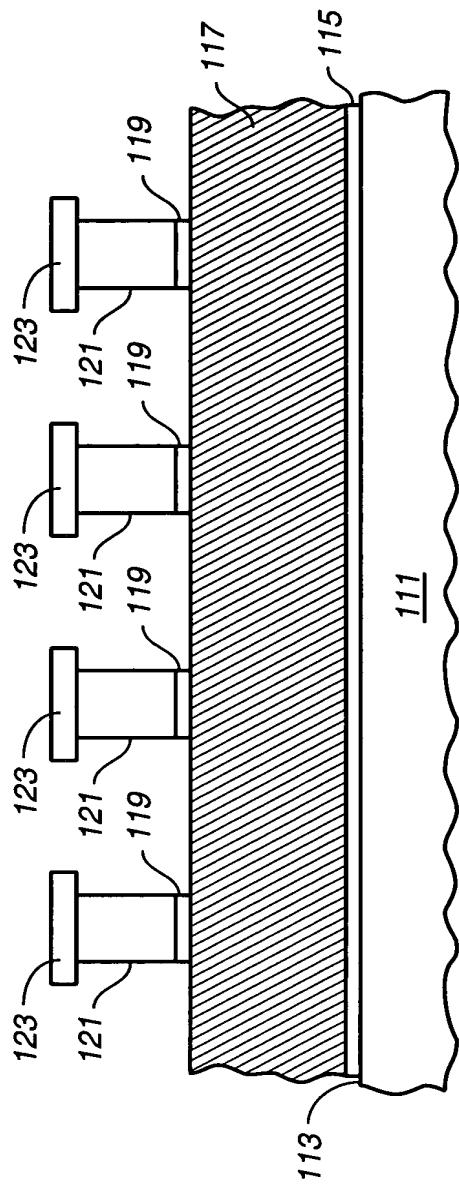


FIG. 6
(Section B-B)

7 / 12



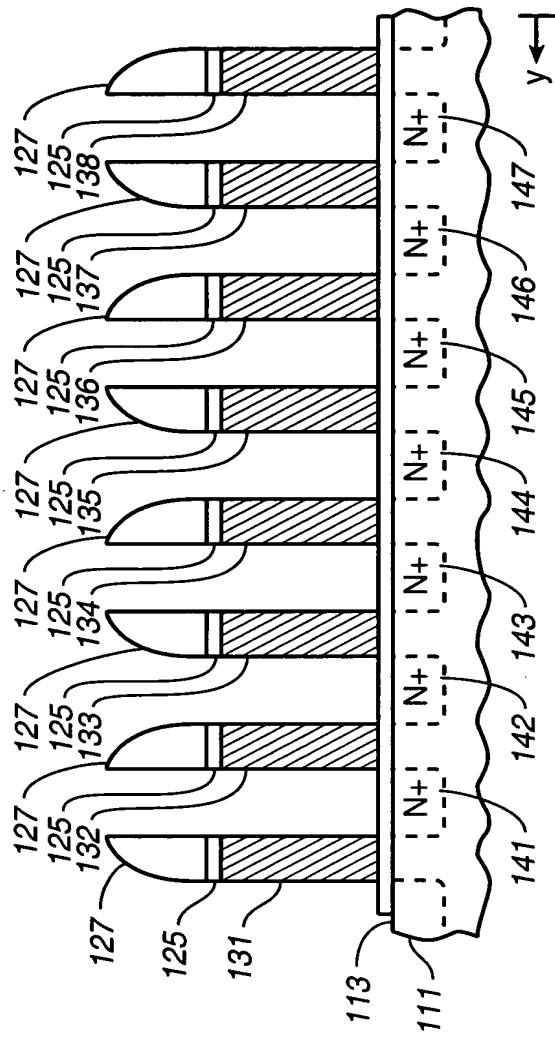


FIG. - 9

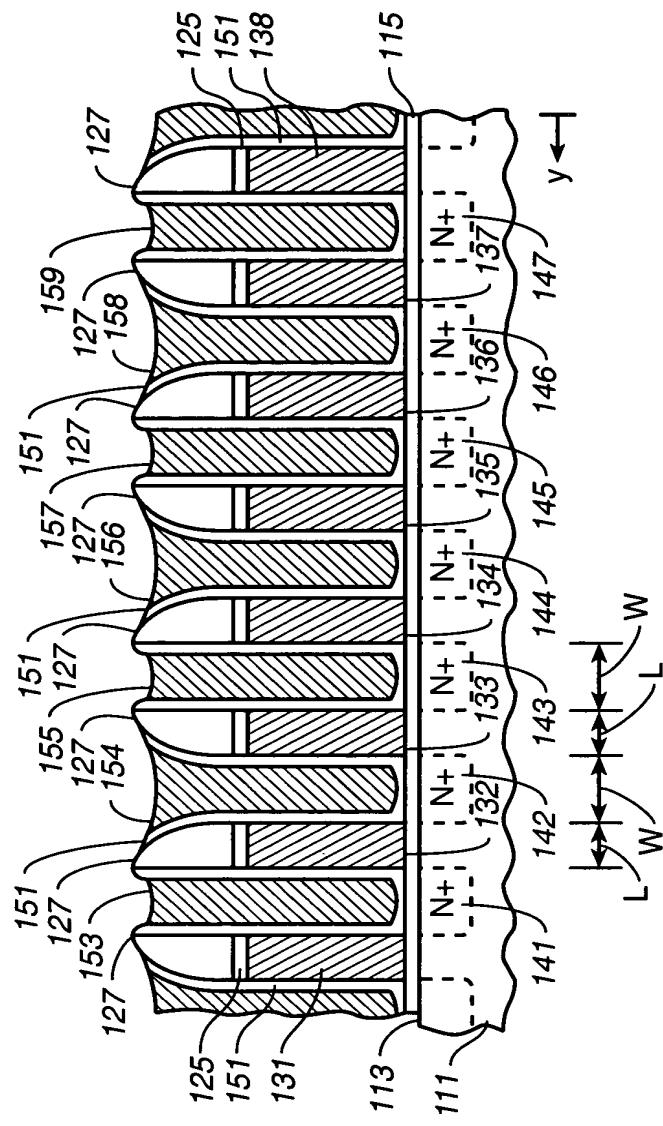


FIG.—10

9 / 12

FIG._11

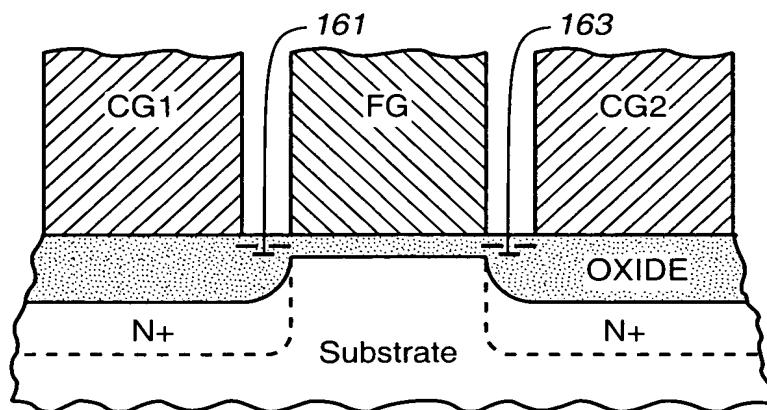


FIG._12

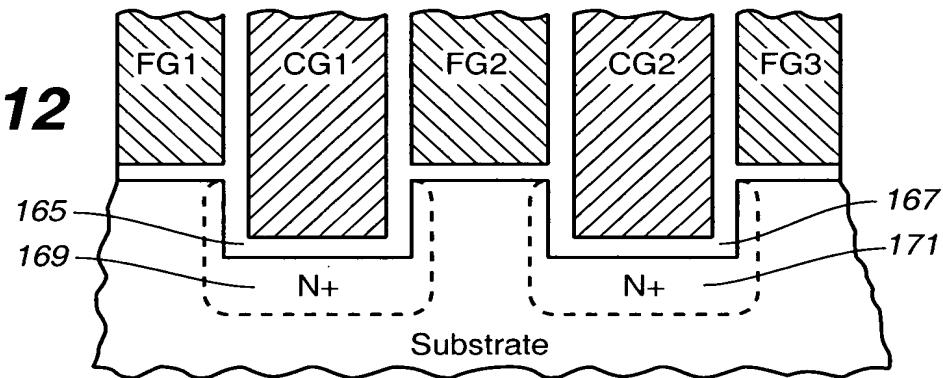
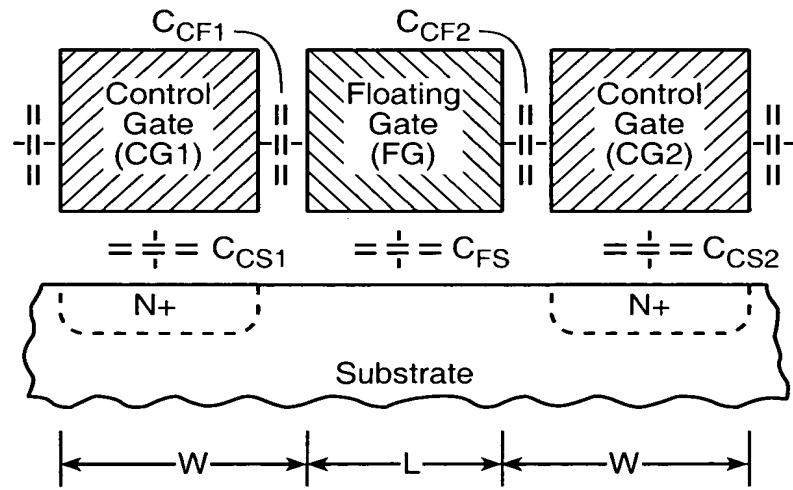


FIG._13



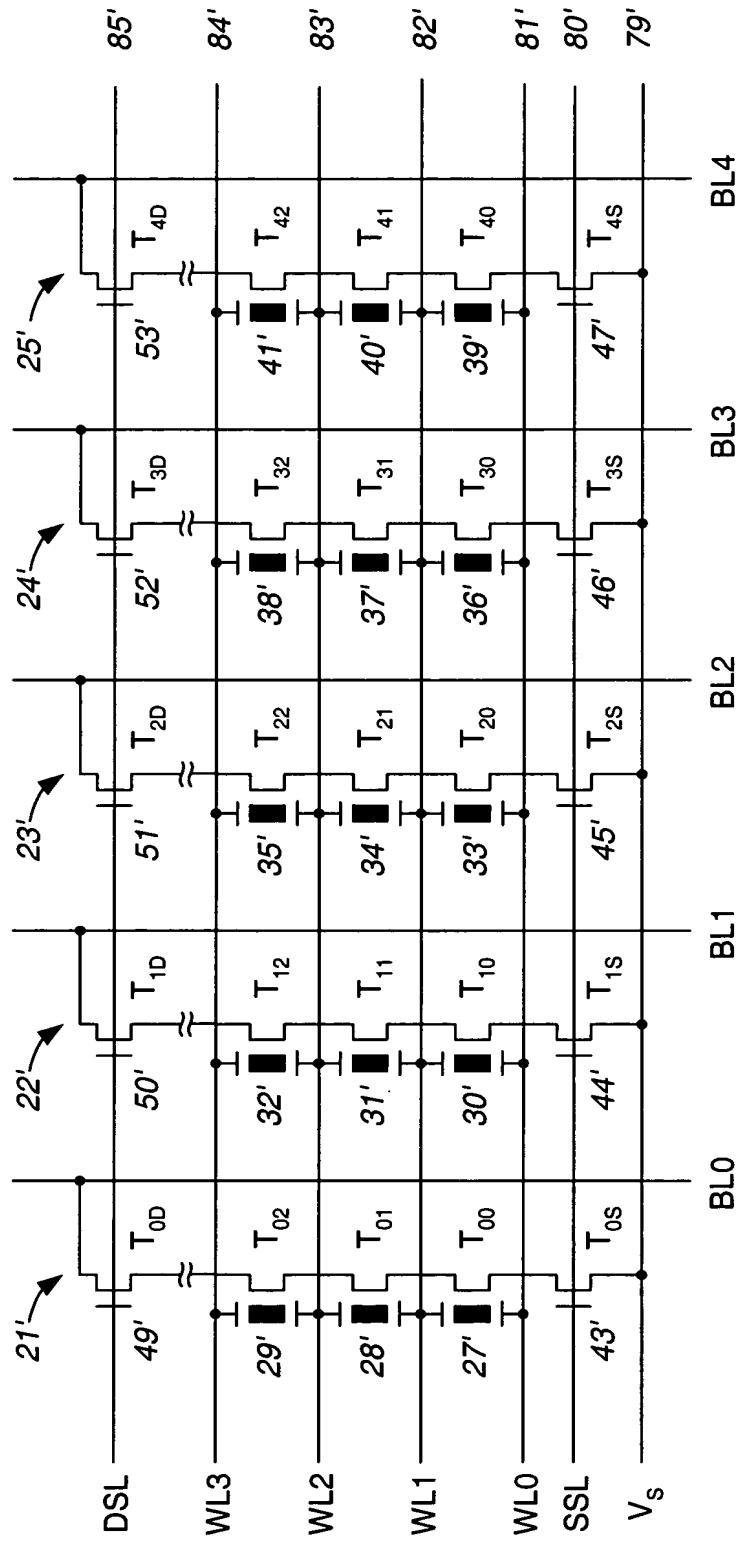


FIG.- 14

	Erase	Program	Read
V_D (bit lines)	Float	Program: 0v Pgm Inhibit: ~2v	sensed
V_{SSL}	Float	~2v	~5v
V_s	Float	0 v, Float, or slight positive	0v
P-Well	~16v	0 v	0v
V_{CG} : (all control gates)	0v - selected block	Float - unselected	-
Selected cell (both gates)	-	~13 - 20 v stepped	0 - 5 v stepped
All unselected cells (above selected cell)	-	~2v	~5v ⁽¹⁾
All unselected cells (below selected cell)	-	~0v	~5v ⁽¹⁾

FIG._ 15

12 / 12



FIG._ 16